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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,910	01/24/2002	Tomoyuki Furuhata	15.58/6459	3803

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,910	FURUHATA, TOMOYUKI	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *03 March 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's Amendment filed 03 March 2003 has been reviewed and placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

2. Claims 1-2, 5-9, and 12-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. U.S. Patent 6,313,537 (patent '537).

Patent '537 discloses in Figures 2-17, particularly Figures 3, 5, 7, and 9, and respective portions of the specification a semiconductor device and method of manufacturing thereof with all limitations as claimed.

Referring to claims 1 and 8 and with reference to Figures 7 and 15a-15c, patent '537 discloses a semiconductor device (and an inherent method of manufacturing thereof) comprising:

a protective insulation layer 338;

a pad opening section 340 provided in the protective insulation layer;

a wiring layer 336 which the pad opening section reaches;

a reflection prevention film (column 10, third paragraph) on at least a portion of the wiring layer 336 that the pad opening section 340 reaches; and

a wiring layer 300/324 provided at a level lower than the wiring layer which the pad opening section reaches,

wherein the wiring layer 300/324 provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

Alternately, referring to claims 1 and 8 and with reference to Figures 9 and 16a-16c, patent '537 discloses a semiconductor device (and an inherent method of manufacturing thereof) comprising:

a protective insulation layer 438;

a pad opening section 440 provided in the protective insulation layer;

a wiring layer 436 which the pad opening section reaches;

a reflection prevention film on at least a portion of the wiring layer 436 that the pad opening section 440 reaches; and

a wiring layer 430/424 provided at a level lower than the wiring layer which the pad opening section reaches,

wherein the wiring layer 430/424 provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

With respect to claims 5, 12, and 17, patent '537 discloses a semiconductor device (and a method of manufacturing thereof) comprising:

a first wiring layer formed above a semiconductor layer 320 and above a first interlayer insulation layer 322;

a second wiring layer 336 that includes a pad section formed above the first wiring layer and above a second interlayer insulation layer 334;

a reflection prevention film (column 10, third paragraph) on at least a portion of the second wiring layer 336;

a protective insulation layer 338 formed above the second wiring layer and the second interlayer insulation layer; and

a pad opening section 340 provided in the protective insulation layer 338,

wherein an upper surface of the first interlayer insulation layer 322 includes a first region where the protective insulation layer is formed vertically thereabove, the first wiring layer is formed on the first region, and no portion of the first wiring layer is formed vertically below the pad opening section 340.

See Figure 9 for a design variation where the first wiring layer is formed on both sides of the device.

Regarding claims 2 and 9, patent '537 further discloses that wiring layer 336 which the pad opening section reaches is composed of one layer.

Referring to claim 6, patent '537 further discloses that the upper surface of the first interlayer insulation layer 322 further comprises a second region where the pad opening section is formed vertically thereabove, and at least part of the second interlayer insulation layer 334 is formed on the second region.

Referring to claim 7, patent '537 further discloses that first wiring layer 300/324 includes a plurality of wiring layers in the same layer, and the plurality of wiring layers 300/324 are formed on the first region.

Referring to claim 13, patent '537 further discloses that the first wiring layer 300/324 is only formed on the first region and the second interlayer insulating layer 334 is formed over the entire second region.

Referring to claim 14, patent '537 further discloses that a portion of the second interlayer insulating layer 334 is formed over the first region.

Referring to claims 15 and 18, patent '537 further discloses that a third wiring layer 300 is positioned between the first wiring layer 324 and the second wiring layer and that a third interlayer insulation layer 328 is positioned between the first interlayer insulation layer 322 and the second interlayer insulation layer 334.

Referring to claim 16, patent '537 further discloses that the third wiring layer 300 is connected to the first wiring layer 324 through a plurality of first plugs 327 and the third wiring layer is connected to the second wiring layer through a plurality of second plugs 333, and the first plugs and the second plugs are positioned to be offset from each other in a vertical direction (column 9, third paragraph).

Referring to claim 19, patent '537 further discloses that no portion of the intermediate lower level wiring layer 328 is disposed vertically below the pad opening section 340.

Referring to claim 20, patent '537 further discloses:

forming the lower level wiring layer to be electrically connected to the intermediate level wiring layer;

forming the intermediate level wiring layer to be electrically connected to the upper level wiring layer;

forming the lower level wiring layer to include a thickness that is less than that of the lower level interlayer dielectric layer;

forming the intermediate level wiring layer to include a thickness that is less than that of the intermediate level interlayer dielectric layer;

forming a plurality of lower level plugs to electrically connect the lower level wiring layer to the intermediate level wiring layer;

forming a plurality of intermediate level plugs to electrically connect the intermediate level wiring layer to the upper level wiring layer; and

wherein the intermediate plugs 333 are formed to be offset from the lower level intermediate plugs 327 in a vertical direction.

3. Claims 1-20, 22, and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Harada et al. U.S. Patent 6,476,491 (patent '491).

Again, because of the huge number of figures involved and the lengthy of the specification, the figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Similar as indicated above in paragraph number 2, patent '491 discloses in Figures 1-13 and respective portions of the specification a semiconductor device and method of manufacturing thereof with all limitations as claimed. Specifically:

Referring to claims 1 and 8 and with reference to Figures 1 and 2A-2K, patent '491 discloses a semiconductor device (and an inherent method of manufacturing thereof) comprising:

a protective insulation layer 27/28;

a pad opening section 29 provided in the protective insulation layer;

a wiring layer 25 which the pad opening section reaches;

a reflection prevention film 25c on at least a portion of the wiring layer 25 that the pad opening section 29 reaches; and

a wiring layer provided at a level lower than the wiring layer which the pad opening section reaches,

wherein the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

With respect to claims 5, 12, and 17, patent '491 discloses a semiconductor device (and a method of manufacturing thereof) comprising:

a first wiring layer formed above a semiconductor layer 1 and above a first interlayer insulation layer 7;

a second wiring layer 25 that includes a pad section 26 formed above the first wiring layer and above a second interlayer insulation layer 22;

a reflection prevention film 25c on at least a portion of the second wiring layer 25;

a protective insulation layer 27/28 formed above the second wiring layer and the second interlayer insulation layer; and

a pad opening section 29 provided in the protective insulation layer 27/28,

wherein an upper surface of the first interlayer insulation layer 7 includes a first region where the protective insulation layer is formed vertically thereabove, the first wiring layer is formed on the first region, and no portion of the first wiring layer is formed vertically below the pad opening section 29.

Note that although throughout the figures only the elements to the left of pad opening are shown, one in the art would recognize that there could be identical elements to the right of the pad opening.

Referring to claims 3 and 10 and referring now to Figure 8, patent '491 further discloses that the wiring layer which the pad opening section reaches is composed of two layers 305/306.

Referring to claims 4 and 11, patent '491 further discloses that the wiring layer which the pad opening section reaches has a thickness that is greater than that of the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches (column 9, second paragraph and column 10, 6th paragraph, "thickness of the tungsten layer 9b is usually about 100

to about 300 nm" and "metal wiring film 25 is generally formed with a thickness of 1.0 .mu.m or more, taking a wire bonding step into account".

Referring to claims 16 and 20 and referring now to Figure 1, patent '491 further discloses:

forming the lower level wiring layer 9 to be electrically connected to the intermediate level wiring layer 13;

forming the intermediate level wiring layer 13 to be electrically connected to the upper level wiring layer 25;

forming the lower level wiring layer 9 to include a thickness that is less than that of the lower level interlayer dielectric layer 10 or 7;

forming the intermediate level wiring layer 13 to include a thickness that is less than that of the intermediate level interlayer dielectric layer 14 or 10;

forming a plurality of lower level plugs 11, 12 to electrically connect the lower level wiring layer 9 to the intermediate level wiring layer 13;

forming a plurality of intermediate level plugs 15, 16 to electrically connect the intermediate level wiring layer to the upper level wiring layer 25; and

wherein the intermediate plugs 15, 16 are formed to be offset from the lower level intermediate plugs 11, 12 in a vertical direction.

Referring to claims 22 and 24-25, patent '491 further discloses that the wiring layer 25 that the pad opening section reaches includes a first portion along the pad opening section 29 and a second portion adjacent to the pad opening section, and wherein the reflection prevention film 25c is located only on the second portion.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

4. Claims 3-4 and 10-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over patent '537 as applied above, and further in view of patent '491.

Patent '537 discloses as claimed a semiconductor device and method of manufacturing thereof but fails to disclose that the wiring layer 436 (Figure 9) which the pad opening section 440 reaches is composed of two layers and that the wiring layer 436 which the pad opening section reaches has a thickness that is greater than that of the wiring layer 424 provided at a level lower than the wiring layer which the pad opening section reaches.

Patent '491 teaches in paragraph 7, column 17 that "by laminating the first pad electrode 305 and the second pad electrode 310 on each other through the via hole 307' having the larger area, it becomes possible to substantially increase the thickness of the pad electrodes. As a result, it becomes possible to prevent the mechanical damage (cracks) of the underlying interlayer insulating film 301 and peeling between the pad electrode and the underlying interlayer insulating layer, even when the power of ultrasonic waves and the compression load are increased in the course of bonding so as to further increase the bonding strength".

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form

the wiring layer 436 (Figure 9) which the pad opening section 440 reaches as being composed of two layers and to form wiring layer 436 which the pad opening section reaches such that the wiring layer 436 has a thickness that is greater than that of the wiring layer 424 provided at a level lower than the wiring layer which the pad opening section reaches. One would have been motivated to make such a modification in view of the suggestion in patent '491 that, just as recited above, thick pad electrode or by forming pad electrode comprising multiple layers, cracks of the underlying interlayer insulating layer and peeling off of the pad electrode could be prevented.

5. Claims 21 and 23-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over patent '537 as applied above, and further in view of Lien U.S. Patent 5,820,926 (patent '926).

Patent '537 discloses as claimed a semiconductor device and method of manufacturing thereof but fails to disclose that wiring layer 436 (Figure 9) that the pad opening section 440 reaches includes a first portion along the pad opening section and a second portion adjacent to the pad opening section, and wherein the reflection prevention film (not shown) is located only on the second portion.

However, it is known in the art, and as is disclosed in patent '926, that to promote bonding of the two adjacent metal layers as in the case of patent '926 and of the bonding wire and the bonding pad as in the case of patent '537, the reflection prevention film (anti-reflection coating – ARC) shall be removed at the interface (column 3, paragraphs 5 and 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form wiring layer 436 that the pad opening section 440 reaches to include a first portion along the pad opening section and a second portion adjacent to the pad opening section such that the reflection prevention film is located only on the second portion and not at the interface (the first portion). One would have been motivated to make such a modification in view of the suggestion in patent '926 that to promote bonding of the two adjacent metal layers or of the bonding wire and the bonding pad as in the case of patent '537, the reflection prevention film shall be removed at the interface, or in other words, the reflection prevention film is located only on the second portion and not at the interface (the first portion).

6. Claims 1-2, 4-6, 8-9, 11-14, and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fujiki et al. U.S. Patent 5,736,791 (patent '791), and further in view of Lien U.S. Patent 5,820,926 (patent '926).

Patent '791 discloses as claimed a semiconductor device and method of manufacturing thereof as detailed in paragraph number 9 of the Office Action dated 20 September 2002, but fails to disclose a reflection prevention film on the wiring layer that the pad opening reaches (Figure 6).

However, it is known in the art, and as is disclosed in patent '926, that to avoid unintentional irradiation in etching process using marks, a reflection prevention film (anti-reflection coating – ARC) is employed between multilayer metal layers, and as in the case of patent '791, between the metal layer for the bonding pad and the bond wire (column 1, lines 22-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a reflection prevention film on the wiring layer that the pad opening reaches. One would have been motivated to make such a modification in view of the suggestion in patent '926 that a reflection prevention film employed between the metal layer for the bonding pad and the bond wire could prevent unintentional irradiation in etching process using marks.

7. Claims 1-2, 5-9, and 12-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Gregoire et al. U.S. Patent 5,939,790 (patent '790) in view of Lien U.S. Patent 5,820,926 (patent '926).

Patent '790 discloses in Figures 2-7 and respective portions of the specification a semiconductor device and method of manufacturing thereof as similarly detailed in paragraph number 2 above, comprising: a top metal interconnection layer substantially covering a pad area, the top metal interconnection layer being electrically connected to a bottom metal interconnection layer at least through bottom metal-filled via holes, characterized in that bottom metal-filled via holes are arranged in a pattern that surrounds the periphery of the pad area.

However, patent '790 fails to disclose a reflection prevention film on the wiring layer that the pad opening reaches. Nevertheless, it is known in the art, and as is disclosed in patent '926, that to avoid unintentional irradiation in etching process using marks, a reflection prevention film (anti-reflection coating – ARC) is employed between multilayer metal layers, and as in the case of patent '790, between the metal layer for the bonding pad and the bond wire (column 1, lines 22-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a reflection prevention film on the wiring layer that the pad opening reaches. One would have been motivated to make such a modification in view of the suggestion in patent '926 that a reflection prevention film employed between the metal layer for the bonding pad and the bond wire could prevent unintentional irradiation in etching process using marks.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (703) 305-0086. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
March 14, 2003

HOAI HO
PRIMARY EXAMINER